CLAIMS

What is claimed is:

1. A semiconductor device including a core and a periphery, the semiconductor device comprising:

a plurality of core gate stacks in the core, each of the plurality of core gate stacks including a first polysilicon gate and a WSi layer above the first polysilicon gate;

a plurality of sources in the core, the plurality of sources residing between a portion of the plurality of core gate stacks; and

a plurality of periphery gates stacks in the periphery, each of the plurality of periphery gate stacks including a second polysilicon gate and a CoSi layer on the second polysilicon gate.

2. The semiconductor device of claim 1 wherein each of the plurality of core gate stacks includes an edge, the semiconductor device further comprising:

a plurality of core spacers, each of the plurality of core spacers residing along an edge of the plurality core gate stacks.

3. The semiconductor device of claim 1 wherein each of the plurality of periphery gate stacks includes an edge, the semiconductor device.further comprising:

a plurality of periphery spacers, each of the plurality of periphery spacers residing along an edge of the plurality periphery gate stacks.

4. The semiconductor device of claim 1 wherein each of the plurality of core gate stacks includes the first polysilicon gate, the WSi layer above the first polysilicon gate, a layer of polysilicon above the WSi layer and a capping layer above the WSi layer.

5. The semiconductor device of claim 4 wherein the capping layer is a SiN layer.

6. The semiconductor device of claim 4 wherein the capping layer is a SiON layer.

7. A method for providing a semiconductor device including a core and a periphery, the method comprising the steps of:

(a) providing a plurality of core gate stacks in the core, each of the plurality of core gate stacks including a first polysilicon gate and a WSi layer above the first polysilicon gate;

(b) providing a plurality of periphery gates stacks in the periphery, each of the plurality of periphery gate stacks including a second polysilicon gate and a CoSi layer on the second polysilicon gate; and

(c) providing a plurality of sources in the core, the plurality of sources residing between a portion of the plurality of core gate stacks.

→ Since the sources are provided so as to reside between portions of the gate stacks, then the stacks need to be formed 1st

{ Invert the order for the Restriction Requirement.

8. The method of claim 7 wherein each of the plurality of core gate stacks includes an edge, the method further comprising the steps of:

(d) providing a plurality of core spacers, each of the plurality of core spacers residing along an edge of the plurality core gate stacks.

9. The method of claim 7 wherein each of the plurality of periphery gate stacks includes an edge, the method further comprising the steps of:

(d) providing a plurality of periphery spacers, each of the plurality of periphery spacers residing along an edge of the plurality periphery gate stacks.

10. The method of claim 9 wherein each of the plurality of core gate stacks includes the first polysilicon gate, the WSi layer above the first polysilicon gate, a layer of polysilicon above the WSi layer and a capping layer above the WSi layer.

11. The method of claim 7 wherein the core gate stack providing step (a) further includes the steps of:

(a1) providing a first polysilicon layer at the core and the periphery;

(a2) providing a first protective layer on the first polysilicon layer;

(a3) removing a portion of the first protective layer at the core;

(a4) providing a WSi layer on the first polysilicon layer;

(a5) providing at least one capping layer on the WSi layer; and

(a6) etching the first polysilicon layer, the WSi layer and the at least one capping layer to form the plurality of core gate stacks.

12. The method of claim 11 wherein the at least one capping layer includes a

second polysilicon layer on the WSi layer and a SiN layer

13. The method of claim 11 wherein the at least one capping layer includes a second polysilicon layer on the WSi layer and a SiON layer

14. The method of claim 11 wherein the periphery is etched down to the first protective layer during the etching step (a6).

15. The method of claim 14 wherein the periphery gate stack providing step (b) further includes the steps of:

(b1) covering the core with a mask;

(b2) etching the first protective layer and the first polysilicon layer at the periphery;

(b3) stripping the protective layer;

(b4) providing the CoSi layer on a remaining portion of the first polysilicon layer at the periphery.